NCS325

50 μV Offset, 0.25 μV/°C, 35 μA, Zero-Drift Operational Amplifier

The NCS325 is a CMOS operational amplifier providing precision performance. The Zero−Drift architecture allows for continuous auto−calibration, which provides very low offset, near−zero drift over time and temperature, and near flat 1/f noise at only 35 μA (max) quiescent current. These benefits make it ideal for precision DC applications. The NCS325 provides rail−to−rail input and output performance and is optimized for low voltage operation as low as 1.8 V and up to 5.5 V. The NCS325 is available in the space−saving SOT23−5 package.

Features

- Low Offset Voltage: 14 μV typ, 50 μV max at 25°C
- Zero Drift: 0.25 μV/°C max
- Low Noise: 1 μVpp, 0.1 Hz to 10 Hz
- Quiescent Current: 21 μA typ, 35 μA max at 25°C
- Supply Voltage: 1.8 V to 5.5 V
- Rail−to−Rail Input and Output
- Internal EMI Filtering
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Current Sensing

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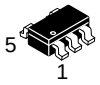
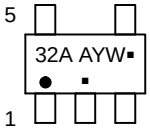
MARKING DIAGRAM

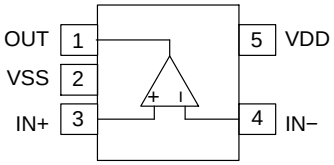


TSOP−5 (SOT23−5) SN SUFFIX CASE 483



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCS325SN2T1G	TSOP−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS

Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage	6	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	(VSS) − 0.3 to (VDD) + 0.3	V
Input Current (Note 1)	±10	mA
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature	−40 to +150	°C
Storage Temperature	−65 to +150	°C
Junction Temperature	−65 to +150	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	4000	V
Machine Model (MM)	200	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input terminals are diode−clamped to the power−supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
2. Short−circuit to ground.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
4. Latch−up Current tested per JEDEC standard: JESD78.

THERMAL INFORMATION

Thermal Metric	Symbol	SOT23−5	Unit
Junction to Ambient (Note 5)	θ_{JA}	235	°C/W

5. As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm^2 and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

OPERATING CONDITIONS

Parameter	Symbol	Range	Unit
Supply Voltage (V_{DD} − V_{SS})	V_S	1.8 to 5.5	V
Specified Operating Range	T_A	−40 to 125	°C
Input Common Mode Voltage Range	V_{ICMR}	V_{SS}−0.1 to V_{DD}+0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Characteristics						
Offset Voltage	V_{OS}	V_S = +5V		14	50	μV
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$	T_A = −40°C to 125°C		**0.02**	**0.25**	μV/°C
Input Bias Current	I_{IB}			±50		pA
Input Offset Current	I_{OS}			±100		pA
Common Mode Rejection Ratio	CMRR	V_{SS}+0.3 < V_{CM} < V_{DD} − 0.3, V_S = 1.8 V	**85**	108		dB
		V_{SS}+0.3 < V_{CM} < V_{DD} − 0.3, V_S = 5.5 V	**90**	110		
		V_{SS}−0.1 < V_{CM} < V_{DD} + 0.1, V_S = 1.8 V		80		
		V_{SS}−0.1 < V_{CM} < V_{DD} + 0.1, V_S = 5.5 V		92		
Input Resistance	R_{IN}			15		GΩ
Input Capacitance	C_{IN}	Differential		1.8		pF
		Common Mode		3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	Output swing within V_{DD}		12	100	mV
Output Voltage Low	V_{OL}	Output swing within V_{SS}		8	100	mV
Short Circuit Current	I_{SC}			±5		mA
Open Loop Output Impedance	Z_{out-OL}	f = 350 kHz, I_O = 0 mA, V_S = 1.8 V		1.4		kΩ
		f = 350 kHz, I_O = 0 mA, V_S = 5.5 V		2.7		
Capacitive Load Drive	C_L			See Figure		
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f_{IN} = 1 kHz		100		nV / $\sqrt{Hz}$
Voltage Noise	e_{P-P}	f_{IN} = 0.01 Hz to 1 Hz		0.3		μV_{PP}
		f_{IN} = 0.1 Hz to 10 Hz		1		μV_{PP}
Current Noise Density	i_N	f_{IN} = 10 Hz		0.3		pA / $\sqrt{Hz}$
Dynamic Performance						
Open Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, V_S = 5.5 V		114		dB
Gain Bandwidth Product	GBWP	C_L = 100 pF, R_L = 10 kΩ		350		kHz
Phase Margin	ϕ_M	C_L = 100 pF		60		°
Gain Margin	A_M	C_L = 100 pF		20		dB
Slew Rate	SR	G = +1, C_L = 100 pF, Vs = 1.8 V		0.10		V/μs
		G = +1, C_L = 100 pF, Vs = 5.5 V		0.16		
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR		100	107		dB
		T_A = −40°C to 125°C	**95**			
Turn−on Time	t_{ON}	V_S = 5 V		100		μs
Quiescent Current	I_Q	No load		21	**35**	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

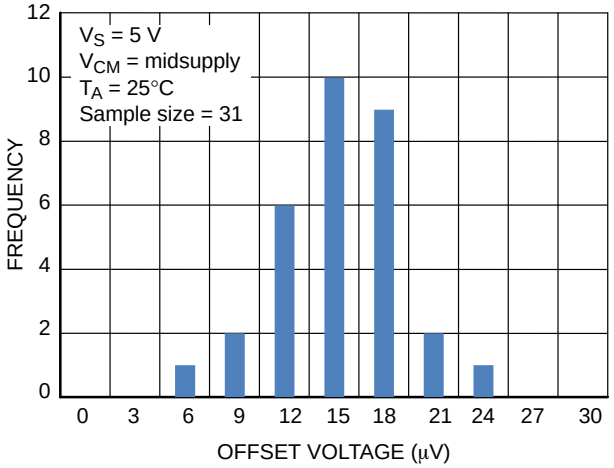


Figure 1. Offset Voltage Distribution

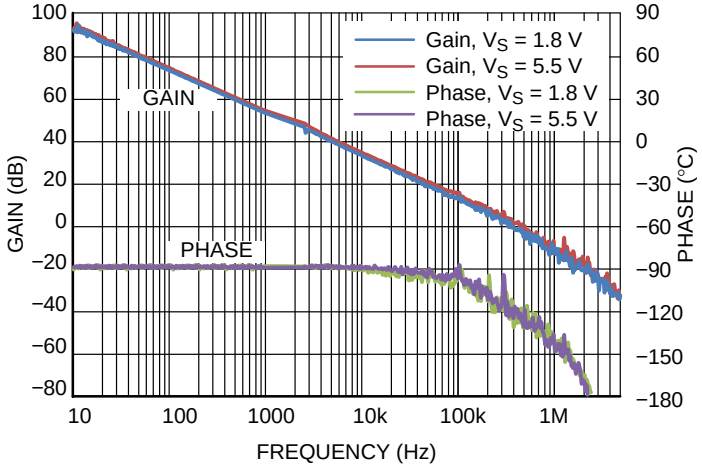


Figure 2. Gain and Phase vs. Frequency

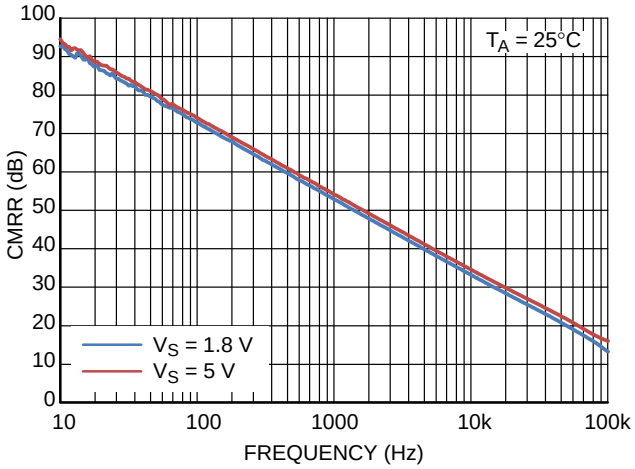


Figure 3. CMRR vs. Frequency

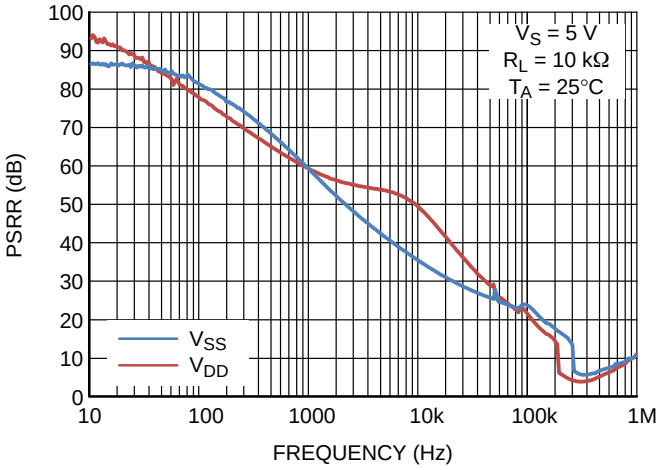


Figure 4. PSRR vs. Frequency

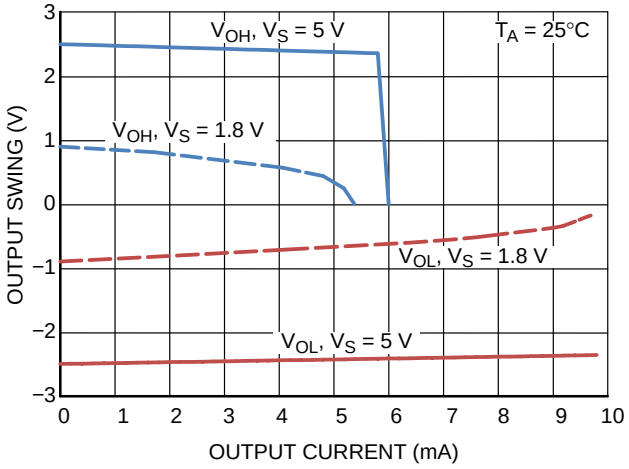


Figure 5. Output Voltage Swing vs. Output Current

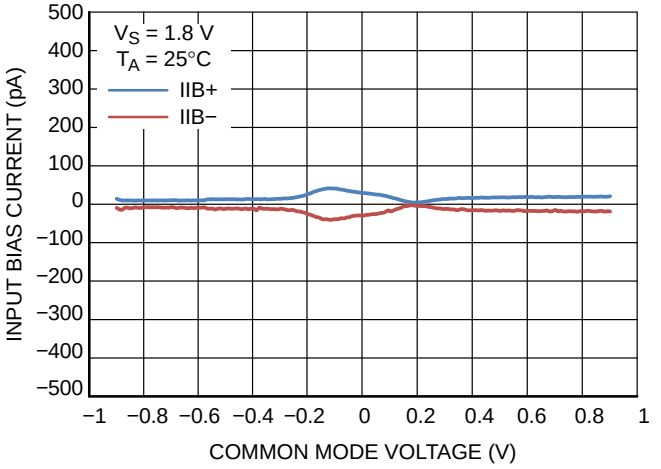


Figure 6. Input Bias Current vs. Common Mode Voltage, V_S = 1.8 V

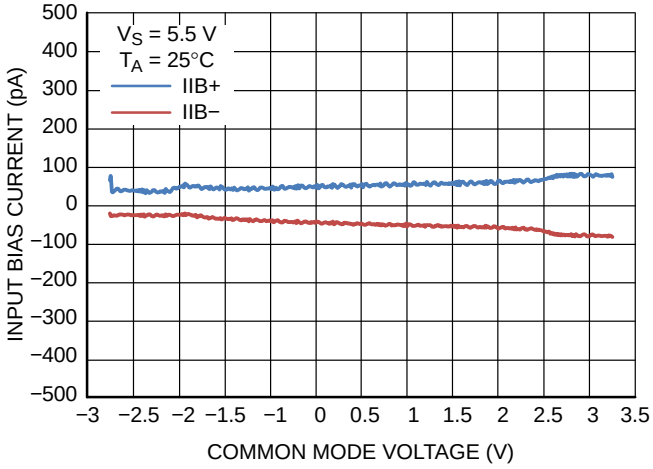


Figure 7. Input Bias Current vs. Common Mode Voltage, V_S = 5.5 V

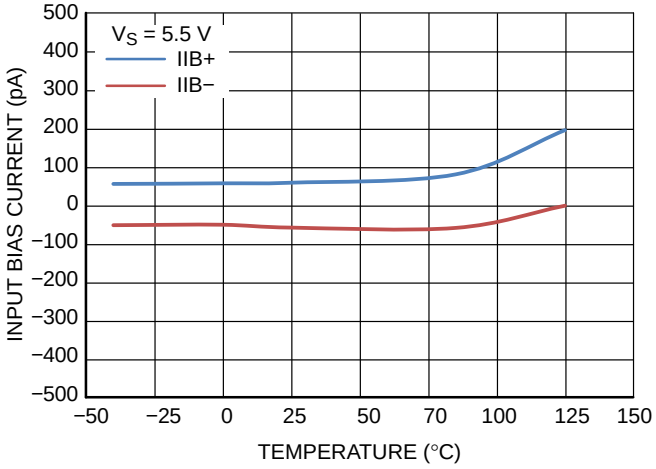


Figure 8. Input Bias Current vs. Temperature

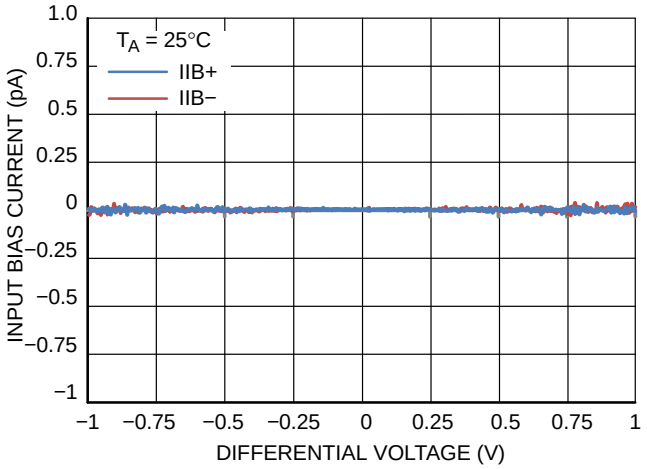


Figure 9. Input Bias Current vs. Input Differential Voltage

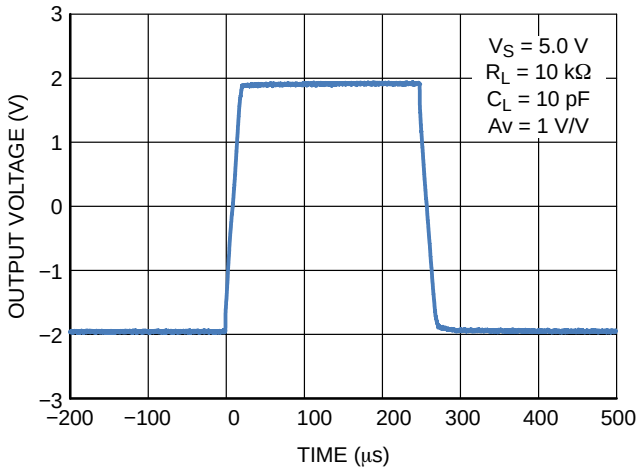


Figure 10. Large Signal Step Response

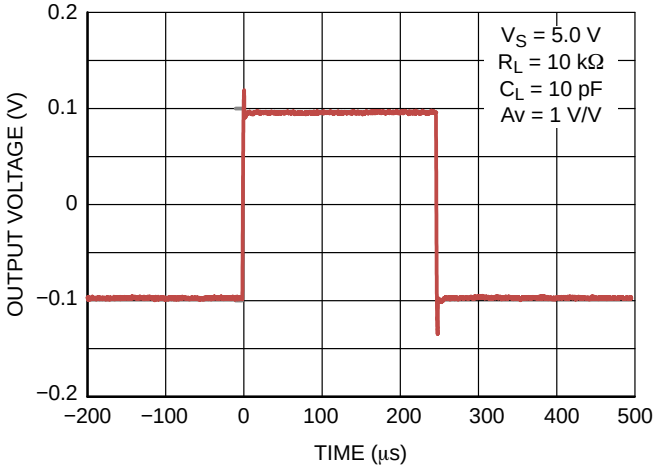


Figure 11. Small Signal Step Response

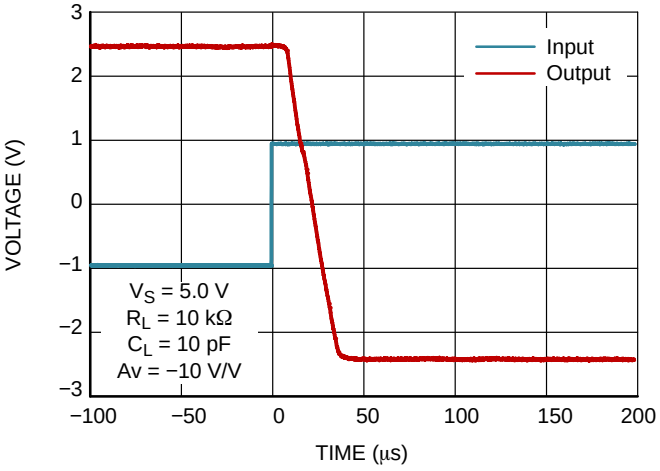


Figure 12. Positive Over Voltage Recovery

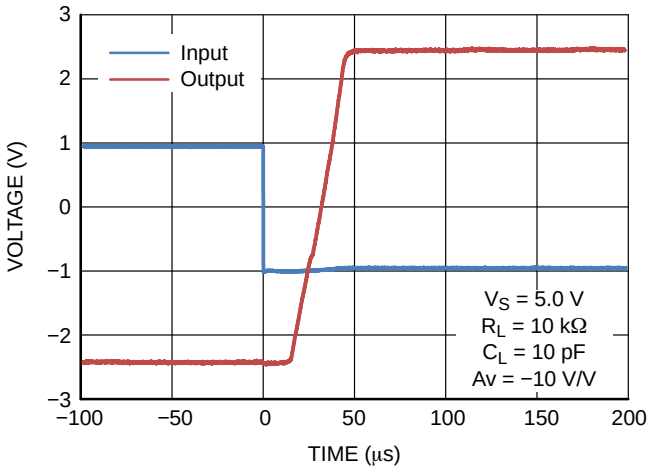


Figure 13. Negative Over Voltage Recovery

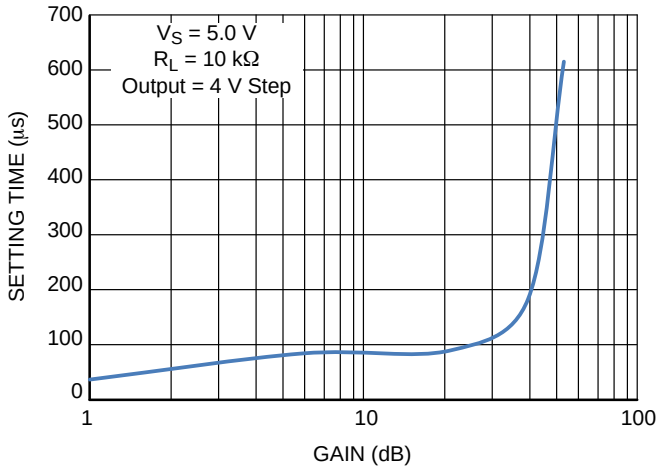


Figure 14. Setting Time vs. Closed Loop Gain

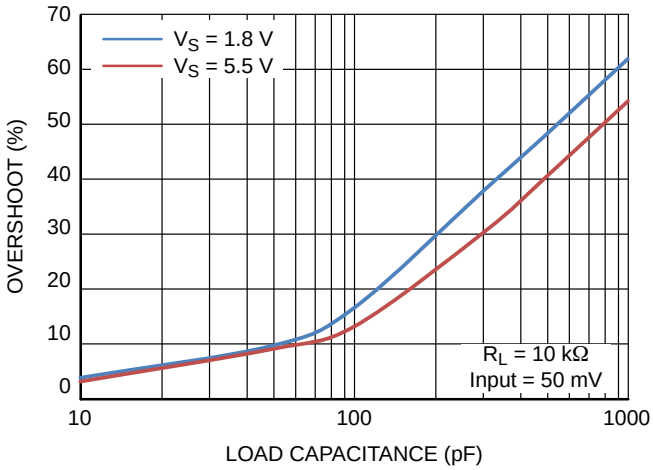


Figure 15. Small Signal Overshoot vs. Load Capacitance

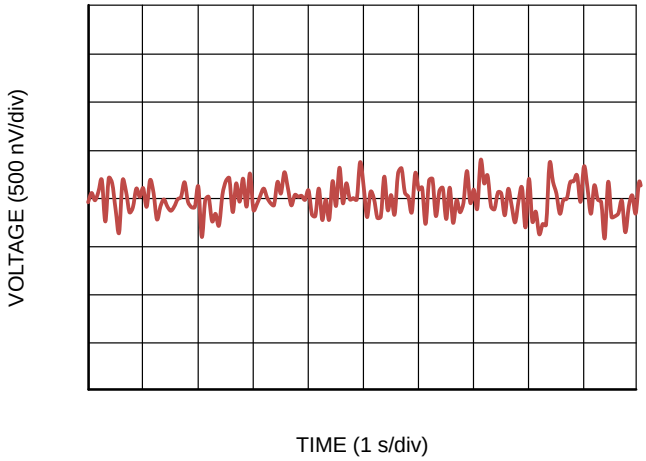


Figure 16. 0.1 Hz to 10 Hz Noise

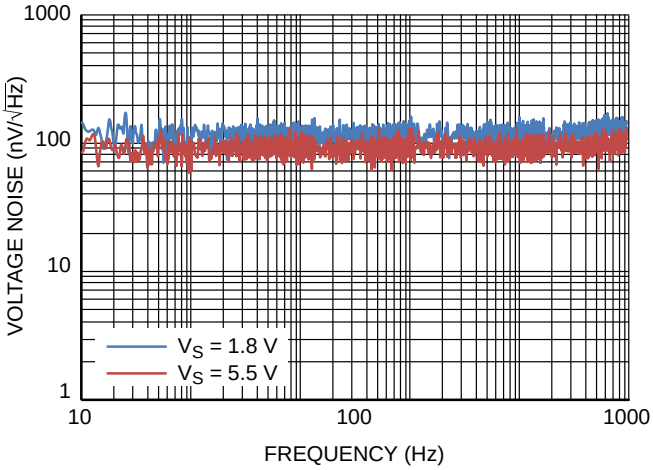


Figure 17. Voltage Noise Spectral Density vs. Frequency

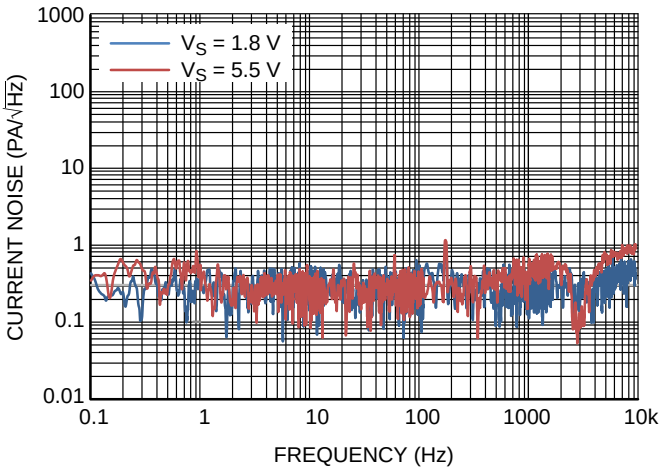


Figure 18. Current Noise Spectral Density vs. Frequency

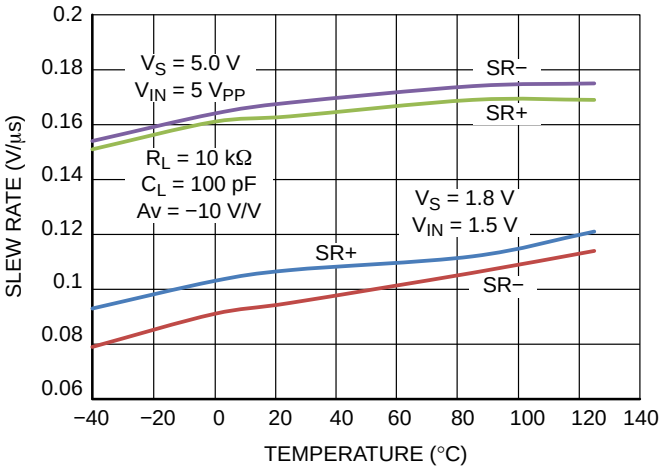


Figure 19. Slew Rate vs. Temperature

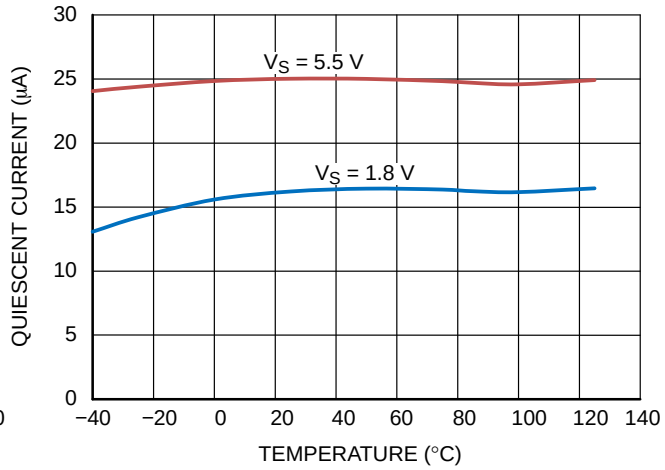


Figure 20. Quiescent Current vs. Temperature

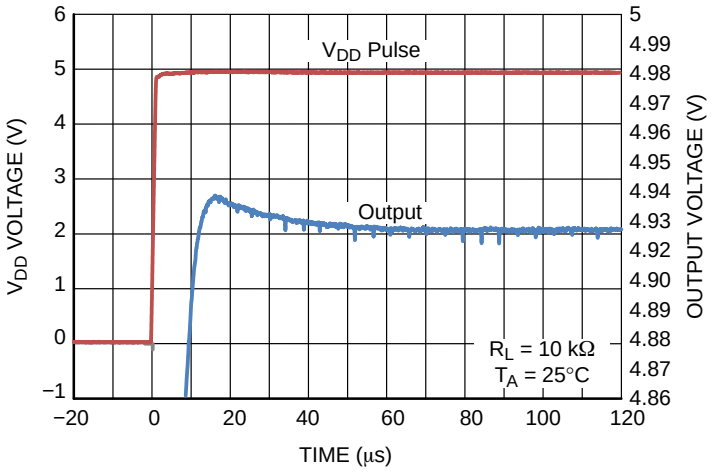


Figure 21. Turn−on Response

APPLICATIONS INFORMATION

OFFSET CORRECTION

The NCS325 uses an auto zero architecture to establish low input offset voltage and noise. With an internal clock of 125 kHz, the amplifier offset is calibrated automatically every 8 μs. The amplifier requires approximately 100 μs to achieve the specified offset voltage.

INPUT VOLTAGE

The NCS325 has a rail−to−rail common mode input voltage range. The typical input bias current of the NCS325 is 50 pA. In an overdriven condition, the output is driven to a supply rail. In this case, the feedback path cannot achieve IN− = IN+. There are no clamp diodes between IN+ and IN− to limit this differential voltage. Diodes between the inputs and the supply rails keep the input voltage from exceeding the rails.

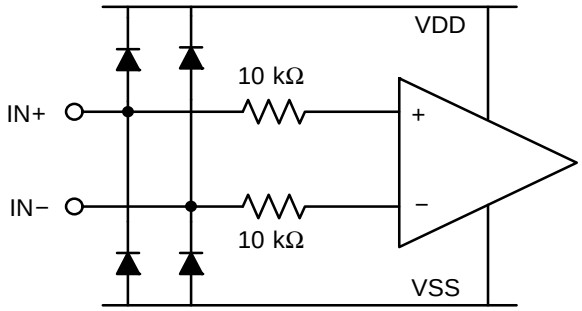


Figure 22. Equivalent Input Circuit

EMI SUSCEPTIBILITY AND INPUT FILTERING

Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI−induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS325 integrates a low−pass filter to decrease its sensitivity to EMI.

APPLICATION CIRCUITS

Low−Side Current Sensing

The goal of low−side current sensing is to detect over−current conditions or as a method of feedback control. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

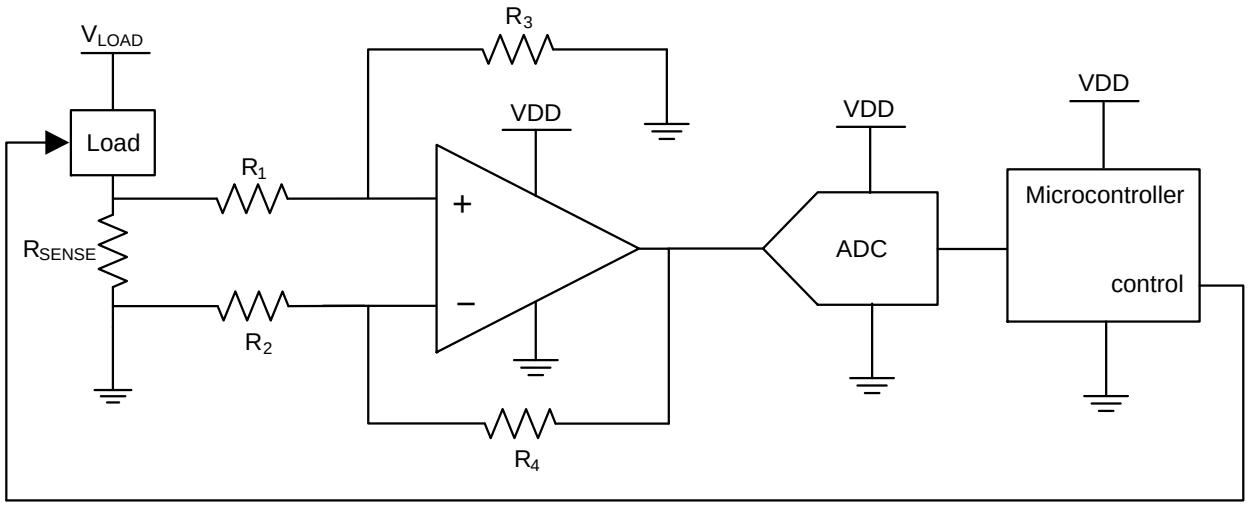


Figure 23. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 24. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

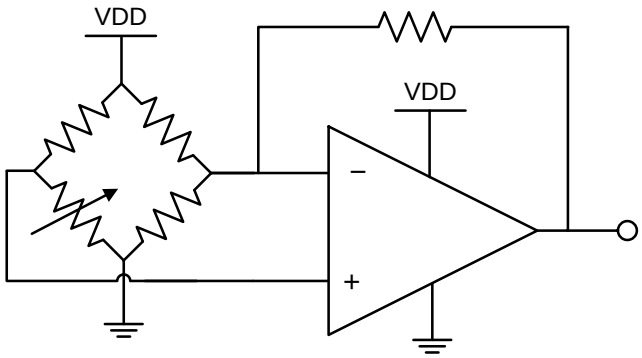


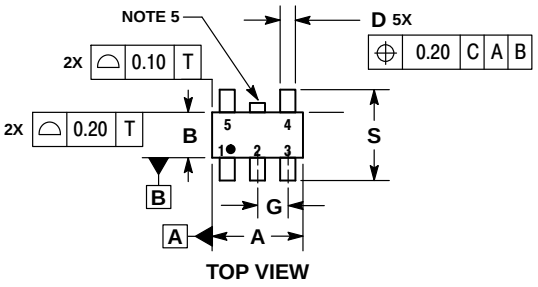
Figure 24. Bridge Circuit Amplification

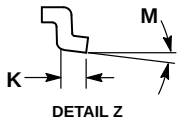
GENERAL LAYOUT GUIDELINES

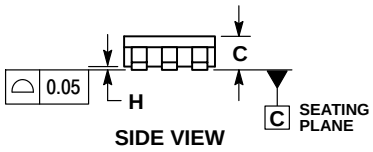
To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric−coefficients and prevent temperature gradients from heat sources or cooling fans.

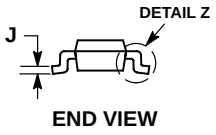
PACKAGE DIMENSIONS

TSOP−5
CASE 483−02
ISSUE K





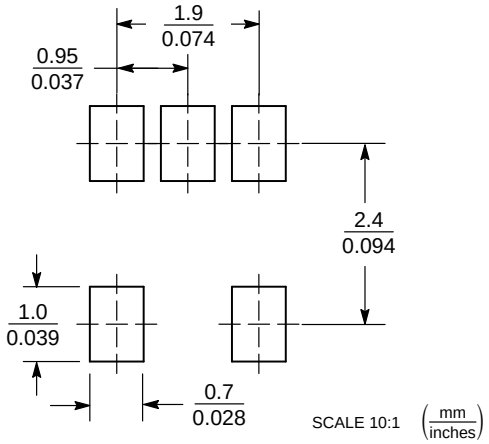




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NCS325/D